**PATENT** 

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Examiner: Not Yet Assigned  Art Unit: Not Yet Assigned				
Kenneth S. McElvain	Art Unit: Not Yet Assigned  ———————————————————————————————————				
Application No.: <u>10/626,031</u>	) FIRST CLASS CERTIFICATE OF MAILING (37 C.F.R. § 1.8(a))  I hereby certify that this correspondence is being deposited with the  United States Postal Service as first class mail with sufficient postage in an envelope addressed to Commissioner for Patents, P.O. Box 1450,				
Filing Date: July 23, 2003	Alexandria, VA 22313-1450 on:				
For: Integrated Circuit Devices and Methods and Apparatuses for Designing Integrated Circuit Devices	S-13-2003 (Date of Deposit)  Dawn R-Shaw (Name of Person Mailing Correspondence)				
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Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450

## INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 together with copies of the documents cited on that form. It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

<u>X</u>	37 C.F.R. §1.97(b).
	37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:
	A statement pursuant to 37 C.F.R. §1.97(e); or
	A check for \$180.00 for the fee under 37 C.F.R. § 1.17(p).
	37 C.F.R. §1.97(d). If so, then enclosed with this Information Disclosure Statement are the following:
	07 O D D 01 07(a), and

- (1) A statement pursuant to 37 C.F.R. §1.97(e); and
- (2) A check for \$180.00 for the fee under 37 C.F.R. §1.17(p) for submission of the Information Disclosure Statement.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated:  $8/12_{-}$ , 2003

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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)					Attorney Docket No.: 02986.P028	Application Number: 10/626,031			
					First Named Inventor: Kenneth S. McElvain				
					Filing Date: July 23, 2003				
	T	MOEMBER		U.S. PATEN	T DOCUMENTS				
Exam. Cite No. 1		U.S. Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
		Number Kind Code <sup>2</sup> (If known)							

		OTHER ART – NO PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published				
		Magma Design Automation, Inc., "Deep-Submicron Signal Integrity", white paper, 2002				
		Andrey V. Mezhiba, Eby G. Friedman, "Scaling Trands of On-Chip Power Distribution Noise", SLIP'02, April 6-7, 2002, San Diego, California, USA, pp.47-53				
		Sani R. Nassif, Onsi Fakhouri, "Technology Trends in Power-Grid-Induced Noise", SLIP'02, April 6-7, 2002, San Diego, California, USA, pp.55-59				
		Seongkyun Shin, Yungseon Eo, William R. Eisenstadt, Jongin Shim, "Analytical Signal Integrity Verification Models for Inductance-Dominant Multi-Coupled VLSI Interconnects", SLIP'02, April 6-7, 2002, San Diego, California, USA, pp.61-68				
		S. Khatri, A. Mehrotra, R. Brayton, A. Sangiovanni-Vincentelli, and R. Otten, "A novel VLSI layout fabric for deep sub-micron applications," in <i>Proceedings of the Design Automation Conference</i> , (New Orleans), June 1999.				
		Sunil P. Khatri, Robert K. Brayton, Alberto Sangiovanni-Vincentelli, "Cross-talk Immune VLSI Design using a Network of PLAs Embedded in a Regular Layout Fabric", IEEE/ACM International Conference on Computer Aided Design, ICCAD-2000, November 5-9, 2000, San Jose, CA, USA				

Examiner		 <del></del>	Γ	Date Considered	
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